UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/993,104	12/18/1997	SCOTT A. ROSENBERG	42390.P5271	4670

7590 09/03/2004

ALOYSIUS T C AUYEUNG
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12TH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 900251206

EXAMINER	
NGUYEN, KIMNHUNG T	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/993,104	ROSENBERG ET AL.	
	Examiner	Art Unit	
	Kimnhung Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Application has been examined. The claims 1-14 and 16-25 are pending. The examination results are as following.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14, and 16-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahara et al. (US Patent 5,436,635) in view of Shields (US Patent 4,870,396).

Regarding claims 1 and 14, Takahara et al. disclose in figure 2, a circuit for modulating voltage signals and associated method comprising: a first circuit configuration (see phase division circuit 42, source drive IC 11/12) to substantially drive respective positive and negative voltage signals (see V (P) and V (M), and a second circuit configuration (TFT as switching elements for writing signal to pixel electrodes, column 6, lines 63-64 to alternately sample the respective voltage signals changeover circuits, column 19, lines 55-65) at a substantially predetermined rate. However, Takahara et al. fail to teach voltage signal storage elements. Shields teaches voltage storage elements (storage capacitors 24, figure 4, column 2, lines 58-63). It would have been obvious to one of ordinary skill in the art at the time of the invention to

utilize the apparatus of Takahara et al. and provide storage capacitors at pixel cell, as taught by Shields to obtain the apparatus Takahara et al. modified by Shields because it would for providing a sample and hold circuit as taught by Shields (column 2, lines 58-60) and facilitate storage of video signal. Note that Takahara et al. teaches first field scanning operation with applied signal V+ and second field scanning operation with applied signal V- (column 14, lines 40-68), the signal written into each pixel electrode changes in polarity (column 14, lines 65-68), the aforementioned TFT as switching elements for writing signal to pixel electrodes operates independently of other TFT; this corresponds to the claimed first circuit adapted to apply the respective positive and negative voltage signals onto the first and second voltage storage elements independently of application of voltage signals to other storage elements.

Regarding claim 2, Takahara et al. modified by Shields teaches liquid crystal cell (Shields, liquid crystal cell shown in figure 4).

Regarding claims 3, 16, Takahara et al. modified by Shields teaches AC driving (Shields, column 1, lines 57-59 implies driving frequency), this corresponds to the claimed substantially at a predetermined rate is related, at least in part to the particular liquid crystal material of the liquid crystal cell.

Regarding claim 4, the circuit of claim 2, wherein said first circuit configuration includes circuitry to address said liquid crystal cell (Shields, transistor 22 shown in figure 4).

Regarding claim 5, wherein said circuit for modulating voltage signals is coupled in a liquid crystal display (LCD system) (Takahara et al., phase division circuit 42 shown in figure 3), said LCD system being adapted to substantially simultaneously (simultaneously operating GIC (P) and GIC (M), Takahara et al., column 19, lines 13-15) and independently drive additional

voltage signals (pplying on-voltage to every other gate signal line, see Takahara et al., column 19, lines 13-15) onto the voltage signals of the respective first and second voltage signal storage elements (see Shields, storage capacitors 24, figure 4, column 2, lines 58-63).

Regarding claim 6, the circuit of claim 2, wherein said second circuit comprises a plurality of transistors coupled to electrically isolate said first and second voltage signal storage elements (see Shields, storage capacitors 24, figure 4, column 2, lines 58-63, from said liquid crystal cell TFT Tp 11 and Tm 11 per pixel cell as shown in figure 1).

Regarding claims 7 and 17, Shield discloses, wherein the first and second voltage storage elements comprise capacitors (Shields, capacitors 24 shown in figure 4).

Regarding claim 8, the circuit of claim 1, wherein said circuit for modulating voltage signals is embodied on an integrated chip (see Takahara et al., column 13, lines 23-35).

Regarding claim 9, Takahara et al. discloses a liquid crystal display system (LCD image projection television system, column 7, lines 41-42) comprising a voltage signal modulation circuit to locally modulate the voltage signal applied across a liquid crystal cell in said LCD system: a first circuit configuration to substantially simultaneously (simultaneously operating GIC (P) and GIC (M), Takahara et al., column 19, lines 13-15) and independently drive respective positive and negative voltage signals (applying on-voltage to every other gate signal line, see Takahara et al., column 19, lines 13-15), (source driver IC(p) 11 and IC(M) 12 shown in figure 2) and a second circuit configuration (TFT as switching elements for writing signal to pixel electrodes, column 6, lines 63-64 to alternately sample the respective voltage signals (see changeover circuits column 19, lines 55-65) at a substantially predetermined rate. However, Takahara et al. fail to teach voltage signal storage elements. Shields teaches voltage storage

elements (storage capacitors 24, figure 4, column 2, lines 58-63). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the apparatus of Takahara et al. and provide storage capacitors at pixel cell, as taught by Shields to obtain the apparatus Takahara et al. modified by Shields because it would provide a sample and hold circuit as taught by Shields (column 2, lines 58-60) and facilitate storage of video signal. Note that Takahara et al. teaches first field scanning operation with applied signal V+ and second field scanning operation with applied signal V- (column 14, lines 40-68), the signal written into each pixel electrode changes in polarity (column 14, lines 65-68), the aforementioned TFT as switching elements for writing signal to pixel electrodes operates independently of other TFT; this corresponds to the claimed first circuit adapted to apply the respective positive and negative voltage signals onto the first and second voltage storage elements independently of application of voltage signals to other storage elements.

Regarding claim 10, Shields discloses the LCD system of claim 9, and further comprising at least one liquid crystal cell coupled to said voltage signal modulation circuit (Shields, liquid crystal cell shown in figure 4).

Regarding claim 11, the LCD system of claim 10, Takahara et al. modified by Shields teaches AC driving (Shields, column 1, lines 57-59 implies driving frequency), this corresponds to the claimed substantially at a predetermined rate is related, at least in part to the particular liquid crystal material of the liquid crystal cell.

Regarding claim 12, the LCD system of claim 10, wherein said system includes circuitry to address said at least one liquid crystal cell (Shields, transistor 22 shown in figure 4).

Regarding claim 13, the LCD system of claim 10, wherein said LCD system is adapted to substantially simultaneously (simultaneously operating GIC (P) and GIC (M), Takahara et al., column 19, lines 13-15) and independently drive additional voltage signals (applying on-voltage to every other gate signal line, Takahara et al., column 19, lines 13-15) onto the respective voltage signals storage elements (Shields, storage capacitors 24, figure 4, column 2, lines 5863).

Regarding claims 18 and 22, Takahara et al. discloses a voltage signal modulation circuit and associated method comprising: a first circuit to substantially simultaneously drive respective voltage signals simultaneously (source driver IC (P) I1 and IC (M) 12 shown in figure 2, simultaneously operating GIC (P) and GIC (M), column 19, lines 13-15); a second circuit to sample the voltage signals (TFT as switching elements for writing signal to pixel electrodes, column 6, lines 63-64 to alternately sample the respective voltage signals (changeover circuits, column 19, lines 55-65). However, Takahara et al. fails to teach voltage signal storage elements. Shields teaches voltage storage elements (storage capacitors 24, figure 4, column 2, lines 58-63). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the apparatus of Takahara et al. and provide storage capacitors at pixel cell, as taught by Shields to obtain the apparatus Takahara et al. modified by Shields because it would for providing a sample and hold circuit as taught by Shields (column 2, lines 58-60) and facilitate storage of video signal.

Regarding claim 19, the voltage signal modulation circuit of claim 18, wherein the voltage signals comprise respective positive and negative voltage signals (source driver IC (P) 1 I and IC (M) 12 shown in figure 2, simultaneously operating GIC (P) and GIC (M), column 19, lines 13-15); and the respective voltage signal storage elements comprise two respective voltage

signal storage elements (since Takahara et al. teach two TFTs Tpl l and Tml l per pixel shown in figure 1, and Shields teaches storage element coupled to switching TFT shown in figure 4) .

Regarding claim 20, the voltage signal modulation circuit of claim 18, wherein said second circuit is adapted to sample the voltage signals of the respective voltage signal storage elements at a substantially predetermined rate (Shields teaches AC driving, column 1, lines 57-59, thus driving frequency).

Regarding claims 21 and 23, the circuit of claim 18, wherein said second circuit is further adapted to sample the voltage signals of the respective voltage signal storage elements (Shields teaches a sample and hold circuit (column 2, lines 58-59) so as to substantially maintain a substantially DC bias.

Regarding claim 24, Takahara et al. discloses a display system (LCD image projection television system, column 7, lines 41-42) comprising a voltage signal modulation circuit to locally modulate the voltage signal applied across a light modulating element in said display system: a first circuit configuration to substantially simultaneously (simultaneously operating GIC (P) and GIC (M), Takahara et al., column 19, lines 13-15) drive respective voltage signals (applying on-voltage to every other gate signal line , Takahara et al., column 19, lines 13-15), (source driver IC(p) 11 and IC(M) 12 shown in figure 2) and a second circuit configuration (TFT as switching elements for writing signal to pixel electrodes, column 6, lines 63-64 to alternately sample the voltage signals (changeover circuits , column 19, lines 55-65) at a substantially predetermined rate. However, Takahara et al. fail to teach voltage signal storage elements. Shields teaches voltage storage elements (storage capacitors 24, figure 4, column 2, lines 58-63). It would have been obvious to one of ordinary skill in the art at the time of the invention was

made to utilize the apparatus of Takahara et al. and provide storage capacitors at each pixel cell, as taught by Shields to obtain the apparatus Takahara et al. modified by Shields because it would for providing a sample and hold circuit as taught by Shields (column 2, lines 58-60) and facilitate storage of video signal. Note that Takahara et al. teaches first field scanning operation with applied signal V+ and second field scanning operation with applied signal V- (see column 14, lines 40-68), the signal written into each pixel electrode changes in polarity (see column 14, lines 65-68), the aforementioned TFT as switching elements for writing signal to pixel electrodes operates independently of other TFT; this corresponds to the claimed first circuit adapted to apply the respective positive and negative voltage signals onto the first and second voltage storage elements independently of application of voltage signals to other storage elements.

Regarding claim 25, the system of claim 24, wherein said system is adapted to drive substantially simultaneously additional voltage signals onto the respective voltage signal storage elements (applying on-voltage to every other gate signal line, Takahara et al., column 19, lines 13-15) onto respective voltage storage elements (Shields, storage capacitors 24, figure 4, column 2, lines 58-63).

Response To Arguments

3. Applicant's arguments filed on 1/2/2004 have been fully considered but they are not persuasive.

Applicant argues that the combination of Takahara et al. and Shields cannot make Applicant's claimed invention, and modification of using the storage elements of Shields would destroy the operation of the device taught by Takahara et al. Examiner respectfully disagrees with the arguments because Takaraha et al. disclose in figure 2, a circuit for modulating voltage

signals and associated method comprising a first circuit configuration (see phase division circuit 42) to substantially drive respective positive and negative voltage signals (see V(P) and V(M), figure 3), and a second circuit configuration (see TFT as switching element signal to pixel electrodes, see column 6, lines 63-64 and column 19, lines 36-38) to alternative sample the respective voltage signals. However, Takahara et al. do not disclose the voltage signal storage elements, Shields discloses the voltage storage elements by storage capacitors (24, see figure 4) as discussed above. Therefore, the combination of Takaraha et al. and Shields are satisfied for its intended purpose. For these reasons, the rejections are maintained.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number (703) 308-0425.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD A HJERPE** can be reached on **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only).

Hand-delivery response should be brought to: Crystal Park II, 2121 Crystal Drive, Arlington, VA Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kimnhung Nguyen
September 2, 2004

RICHARD HJERPE 9/2/04
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600